

**6162A  
TOTALIZER**

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## TABLE OF CONTENTS

		PAGE
1.0	GENERAL INFORMATION	1
2.0	SPECIFICATIONS	1
2.1	Main Assembly	1
2.2	Signal Conditioning	2
3.0	MECHANICAL ASSEMBLY AND INSTALLATION	5
3.1	Unpacking and Inspection	5
3.2	Safety Considerations	5
3.3	Panel Mounting Procedure	6
4.0	POWER AND SIGNAL INPUT CONNECTIONS	7
4.1	AC Power Connections	7
4.2	Changing Operating Voltage	8
4.3	DC Power Connections	9
4.4	Signal Input Connections	9
4.5	RESET Connection	9
5.0	OPERATING INSTRUCTIONS	10
5.1	Main Board Connector, P1	11
5.2	Up/Down Selection	11
5.3	Decimal Points	12
5.4	Signal Conditioning	13
5.5	Counting Edge	14
5.6	Predivider Option	14
5.7	Display and Overload Indications	15
6.0	EXCITATION SUPPLY CONNECTIONS	15
6.1	NAMUR Transducer Connection	17
7.0	PARALLEL BCD OUTPUT OPTION (F6)	18
7.1	Parallel BCD Output Specifications	19
7.2	BCD Output Connections	20
7.3	BCD Configuration Selection	21
7.4	BCD HOLD and DATA READY	27
7.5	HANDSHAKING DETAILS	27
8.0	DRAWINGS	29

ILLUSTRATIONS	PAGE	
Figure 3-1	Exploded View of Meter and Case	6
Figure 4-1	Rear View of Case With F6 Option Connector	7
Figure 4-2	Side View of Transformer	8
Figure 5-1	Board Interconnections	10
Figure 5-2	Display Board Jumper Locations	12
Figure 5-3	Signal Conditioner Jumper Locations	13
Figure 6-1	Main Board Jumper Locations	16
Figure 6-2	NAMUR Transducer Configuration	17
Figure 7-1	BCD Output Jumper Locations	21
Figure 8-1	6162A Main Assembly Diagram	29
Figure 8-2	6162A Schematic Diagram (1 of 3)	30
Figure 8-3	6162A Schematic Diagram (2 of 3)	31
Figure 8-4	6162A Schematic Diagram (3 of 3)	32
Figure 8-5	Signal Conditioner Assembly Diagram (with PD Option)	33
Figure 8-6	Signal Conditioner Schematic Diagram (with PD Option)	34
Figure 8-7	Parallel BCD Assembly Diagram	35
Figure 8-8	Parallel BCD Schematic Diagram	36
Table 5-1	Binary Values of Jumper Positions	14
Table 7-1	BCD Address Configuration	22

## 1.0 GENERAL INFORMATION

The Model 6162A is a 6-digit up-down totalizer for applications up to 999,999 counts. Bi-directional totalising is achieved with a count input and an Up/Down control input. However, counting below zero (negative values) is not possible except in the 10's complement form (e.g. -3 is displayed as 999997). Reset can be remote or with a front-panel pushbutton.

The standard meter includes a main board which contains the counters, power supply and display. A signal conditioner is provided with all units as standard which may be configured to accommodate various types of signals. A transducer excitation supply is provided for powering inductive proximity switches and photoelectric sensors. A high gain input accommodates passive inductive pickups.

Options for the totaliser are a 1-255 programmable predivider to provide engineering units and a parallel BCD output board. On special order, the predivision can be increased up to a maximum of 4095. The user-adjustable jumper switch will be able to increase the factory-installed predivision (3840 max.) from 0 to 255 in steps of 1. Refer to section 5.6 for more details.

## 2.0 SPECIFICATIONS

### 2.1 MAIN ASSEMBLY

#### Display:

Display type	7 segment, red LED
Digit height	14.2 mm (0.56 inch)
Symbols	8.8.8.8.8.8.
Leading zero blanking	2 most-significant-digits
Decimal points	Five positions, programmable by jumper
Overflow indication	Single LED lamp indicates count has exceeded capacity

#### Power input:

Standard AC power voltage	120 or 240 VAC +10%/-15%
AC frequency range	49 to 440 Hz
Optional DC voltage	5 V $\pm$ 5% (non-isolated)
Optional DC voltage	9-32 or 26-56 VDC, isolated to 300 Vp
Optional AC voltage	24 VAC $\pm$ 10%
Power consumption	5 W max

Excitation supplies:

All options	+5 VDC $\pm$ 5% (1k source impedance)
Excitation voltage	
(Power options except C3)	12 V at 20 mA, 24 V at 30 mA max
(Power option C3)	12 V at 20 mA, 18 V at 22 mA max

Common Mode Voltage:

AC powered,	
Sig Gnd to Pwr Gnd	1500 Vp per HV test; 354 Vp per IEC spacing
DC powered,	
Sig Gnd to DC Pwr Return	300 Vp
	(Except 5 VDC models, non-isolated)

Environmental:

Operating temperature	0 to 50°C
Storage temperature	-40 to +85°C
Relative humidity	To 95%, non-condensing

Mechanical:

Dimensions	Newport DIN2A (short 1/8 DIN) case
Bezel	96 x 48 x 5.1 mm (3.78 x 1.89 x 0.2 in)
Depth behind bezel	104 mm (4.09 in)
Panel cutout	92 x 45 mm (3.62 x 1.77 in)
Weight nominal	300 g (11 oz)
Case material	94V-0 UL-rated polycarbonate

Connectors:

Main board assembly	Single row, 18 pin solder-eyelet (D1 option)
Power and signal	Screw terminal barrier strip (standard)

## 2.2 SIGNAL CONDITIONING

AC\* Signal input:

Minimum signal	10 mV rms at DC-60 Hz 200 mV rms at 10 kHz; 500 mV rms at 20 kHz
----------------	--

\*NOTE: There is no blocking capacitor in series with either the AC or DC inputs. If the input signal has a large DC voltage component, an external blocking capacitor (e.g. 0.22 microfarad, 200 v) should be placed between the signal and TB1-5; a resistor (e.g. 100 k Ohms) should be connected between TB1-5 and TB1-4 and finally, TB1-6 should be connected to TB1-4. The capacitor should not be connected to TB1-6 due to the small negative limitation (-0.6 V) of that input.

Switching threshold  
(typical, with S3-C  
jumper not used)

+8 mVDC with 6 mVp-p hysteresis, DC to 60 Hz  
or 8 mV rms with 0 mVDC DC to 60 Hz

+8 mVDC with 35 mVp-p hysteresis, at 10 kHz  
or 54 mV rms with 0 mVDC at 10 kHz

Maximum signal  
Overload protection  
Input resistance

+8 mVDC with 63 mVp-p hysteresis at 20 kHz  
or 123 mV rms with 0 mVDC at 20 kHz  
30 V rms  
240 VAC  
Greater than 100 kOhm at low frequencies  
100 kOhm (above 10 kHz)

DC Signal input:

DC (high level)

Signal input (TB1-6):

Switching threshold  
Maximum signal  
Input resistance  
Frequency response  
(for a 0 to +5 V,  
50% square wave)

+1.65 V typ. with a 0.26 V typ. hysteresis  
-0.6 and +50 VDC  
11 kOhm pull-up resistor to +5 V  
90 Hz or 9,000 Hz (jumper-selectable)

DC Contact Closure input (TB1-6):

Voltage source  
Switching threshold  
Maximum signals  
Input resistance  
Frequency response  
(50% duty cycle contact  
closure or open-collector  
NPN transistor input)

Internal +5 V with 11 kOhm resistance  
+1.65 V typ. with a 0.26 V typ. hysteresis  
-0.6 and +50 VDC  
11 kOhm pull-up resistor to +5 V  
80 Hz or 8,000 Hz (jumper-selectable)

Reset input:

RESET

TB1-7 or P1-S

There is a 4.53 kOhm pull-up resistor to +5 V and a pull-up current source of from 0.01 mA to 0.20 mA.

Logical '0'  
(this resets  
the counter)

0.0 V to +0.7 V OR

contact closure to digital gnd. (P1-T) OR  
contact closure to signal gnd.\* (TB1-4) OR  
by pressing the front panel pushbutton OR  
by applying a TTL logic "0" level voltage  
(referenced to digital gnd. - P1-T).

Logical '1'

+2.4 V to +4.75 V OR

opening the contact OR  
by releasing the front panel pushbutton OR  
by applying a TTL logic "1" level voltage  
(reference to digital gnd. - P1-T).

Count direction input

UP/DOWN

P1-V

There is a 4.75 kOhm pull-up resistor to +5 V and a pull-up current source of from 0.01 mA to 0.20 mA.

Logical '0'  
(this causes the  
counter to count down)

0.0 V to +0.7 V OR

contact closure to digital gnd. (P1-T) OR  
contact closure to signal gnd.\* (TB1-4) OR  
by applying a TTL logic "0" level voltage  
(reference to digital gnd. - P1-T).

Logical '1'  
(this causes the  
counter to count up)

+2.4 V to +4.75 V OR

opening the contact OR  
by applying a TTL logic "1" level voltage  
(reference to digital gnd. - P1-T).

Input Predivider: (PD Option)

Setability

Programming method

Integers from 1 to 255

Internal push-on jumpers

\*NOTE: When the input signal (to be counted) is very small in magnitude, it may be preferable not to use signal gnd. for this digital circuit return path.

## 3.0 MECHANICAL ASSEMBLY AND INSTALLATION

### 3.1 UNPACKING AND INSPECTION

Your digital panel meter was systematically inspected and tested, then carefully packed before shipment. Unpack the instrument and inspect it for shipping damage. Notify the freight carrier immediately if damage exists.

Each package includes: an assembled meter, an owners manual, and any additional options ordered. If any items are not according to your order, contact your local distributor or Newport Electronics.

### 3.2 SAFETY CONSIDERATIONS

This instrument complies with required safety regulations. To prevent electrical or fire hazard and ensure safe operation, please follow these guidelines.

**VISUAL INSPECTION:** Do not attempt to operate the instrument if damage is found.

**MOUNTING:** This instrument is designed for mounting in a metal panel. Check the dimensions of the panel cutout and observe the mounting instructions.

**POWER VOLTAGE:** This instrument is delivered with the AC power input connected for 240 VAC in Europe (C1 option) or 120 VAC in the USA (unless the instrument is provided with the DC power input option). Verify that the instrument is connected for the correct power voltage rating before using. If incorrect, make the required change as described in Changing Operating Voltage (Section 4.2).

**POWER WIRING:** This instrument has no power switch; it will be in operation as soon as the power is connected.

Verify that the power cable has the proper ground (earth) wire and that this wire is properly connected to an adequate ground (earth) point. The meter must be grounded (earthed) in accordance with the latest local safety regulations.

This instrument is protected according to Class I (Protective Earth) of the IEC (International Electrotechnical Commission) 348 and VDE 0411 regulations. If AC, the power cable must contain a protective ground (earth) conductor which is not disconnected (open) either inside or outside the instrument. No extension cables without grounding (earthing) wires shall be used.

**SIGNAL WIRING:** Do not make signal wiring connections or changes while power is on. Make signal connections before power is applied. If connection changes are required, first disconnect the power.

**RAIN OR MOISTURE:** Do not expose the instrument to condensing moisture.

**FUMES AND GASES:** Do not operate the instrument in the presence of flammable gases or fumes; such an environment constitutes a definite safety hazard.

**EXERCISE CAUTION:** As with any electronic instrument, high voltages may be exposed when attempting to install, calibrate, or remove parts of the meter.

### 3.3 PANEL MOUNTING PROCEDURE

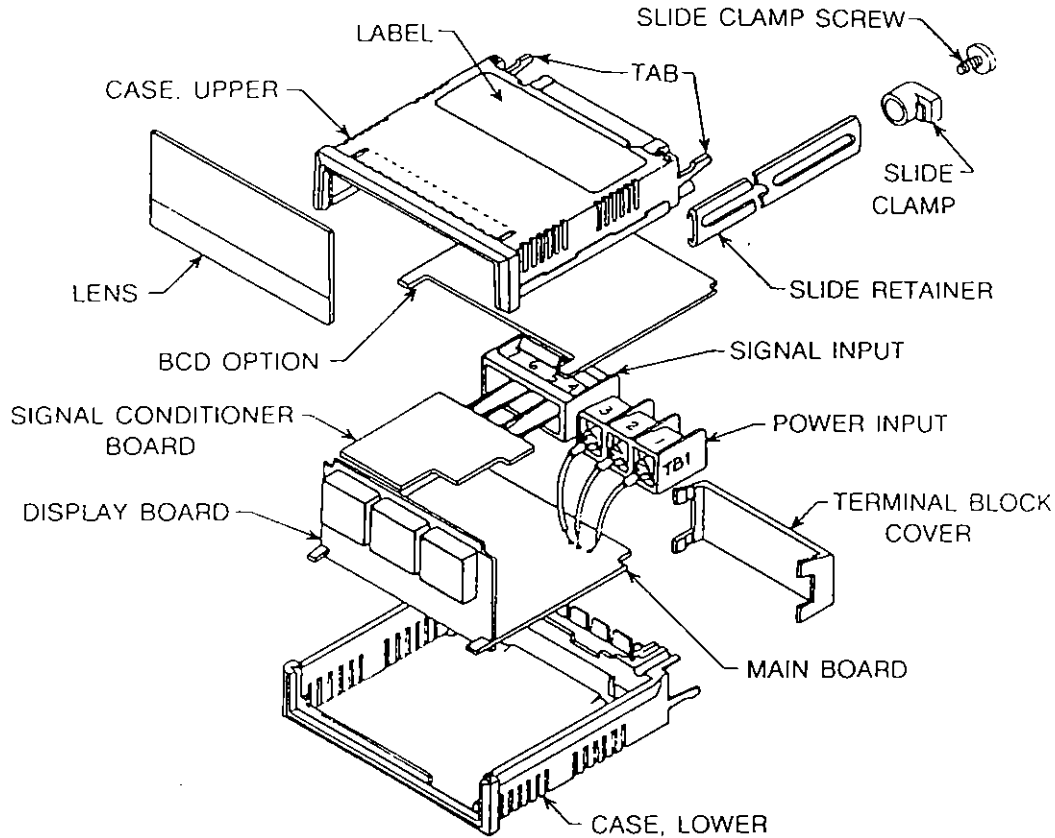


Figure 3-1 Exploded View of Meter and Case

1. Remove main board edge connector P1 option, if installed.
2. Loosen the two clamp screws (with a #8 Phillips screwdriver) until they can be rotated.
3. Push the two slide retainers toward the rear of the case, and remove them.
4. Insert the meter into the panel cutout, working from the front.
5. Insert the slide retainers back onto the case, and push them up tightly against the rear of the panel.
6. Rotate slide clamps back into original position and tighten clamp screws just enough to hold the case in place. NEVER OVERTIGHTEN CLAMP SCREWS.
7. Install any connectors that have been removed.

## 4.0 POWER AND SIGNAL INPUT CONNECTIONS

Refer to the safety considerations in the previous section prior to connecting the power. Figure 4-1 identifies the connectors and screw terminal barrier (TB1), and their respective terminal numbers or letters. Refer to this figure when making power and signal connections.

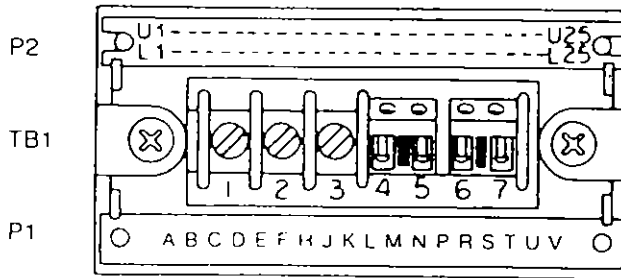


Figure 4-1 Rear View of Case With F6 Option Connector and Main Board Connector

### 4.1 AC Power Connections (dependent on option)

The 6162A meter is configured by Newport or its authorized distributors for 240 VAC operation in Europe and 120 VAC in the USA.

To change the meter from 240 VAC to 120 VAC operation, refer to Section 4.2.1, Changing Operating Voltage. To change the meter from 120 VAC to 240 VAC operation, reverse the procedure of Section 4.2.2.

AC POWER CONNECTIONS VIA TERMINAL BARRIER TB1			
TB1 Terminals	Power Operation	Wire Colour	
		USA	Europe
1	AC Power HI	Black	Brown
2	AC Power LO	White	Blue
3	AC Power GND	Green	Green/Yellow

## 4.2 CHANGING OPERATING VOLTAGE

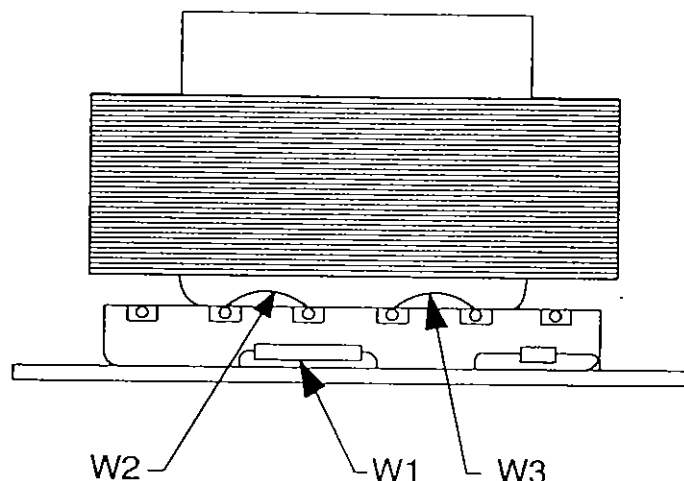


Figure 4-2 Side View of Transformer

Power Line Voltage	Install	Remove
120 V 240 V	W2, W3 W1	W1 W2, W3

### 4.2.1 240 VAC to 120 VAC

To change the meter in the field from 240 VAC to 120 VAC operation, follow this procedure:

1. Remove power connections to the meter, then remove the meter from the case.
2. Refer to Figure 4-2. Remove jumper W1 on the printed circuit board.
3. Add jumpers W2 and W3 on the transformer. The meter is now wired for 120 VAC

### 4.2.2 120 VAC to 240 VAC

To change the meter from 120 VAC to 240 VAC operation, reverse the above procedure in steps 2 and 3.

### 4.3 DC POWER CONNECTIONS

When the 6162A is ordered with a DC power option, it is configured by Newport or its authorized distributors for 5 VDC, 9 - 32 VDC or 26 - 56 VDC operation. Make the power connections shown below.

None of the above DC options can be converted to perform the function of another. Different static inverters must be installed by Newport or its distributors.

DC POWER CONNECTIONS VIA TERMINAL BARRIER TB1	
TB1 Terminals	DC Power Connections
1	No Connection
2	DC Power Plus (+)
3	DC Power Minus (-)

### 4.4 SIGNAL INPUT CONNECTIONS

The 6162A uses terminals 4, 5 and 6 of the barrier strip TB1 for signal inputs (Figure 4-1). Connections should be made before power is applied to the unit. The signal inputs are suitable for AC signals without DC components, DC signals and DC contact closures.

TB1 Terminals	Signal
4	Common (signal gnd.)
5	AC Signal Input
6	DC Signal Input
7	RESET Input

\*NOTE: It is important to connect the unused Signal Input (5 or 6) to common for proper operation

### 4.5 RESET CONNECTION

Totaliser reset is achieved by momentary connection of TB1 terminal 7 to TB1 terminal 4 or logic level 0 to TB1 terminal 7 (or front-panel pushbutton). Totaliser reset is also achieved by the momentary connection of P1-pin S to P1-pin T or a logic level 0 to P1-pin S.

## 5.0 OPERATING INSTRUCTIONS

The 6162A consists of a lower main board and a signal conditioner board. As an option, it may contain a Parallel BCD (F6) upper board. The meter is configured by placing push-on jumpers on these boards according to the instructions of this manual. These boards are accessed by disassembling the meter as illustrated in the exploded view of Figure 3-1. The mezzanine (signal conditioner) and upper boards contain flexible cables that plug into two connectors on the main board as shown in Figure 5-1.

UPPER BOARD

MEZZANINE BOARD

MAIN BOARD

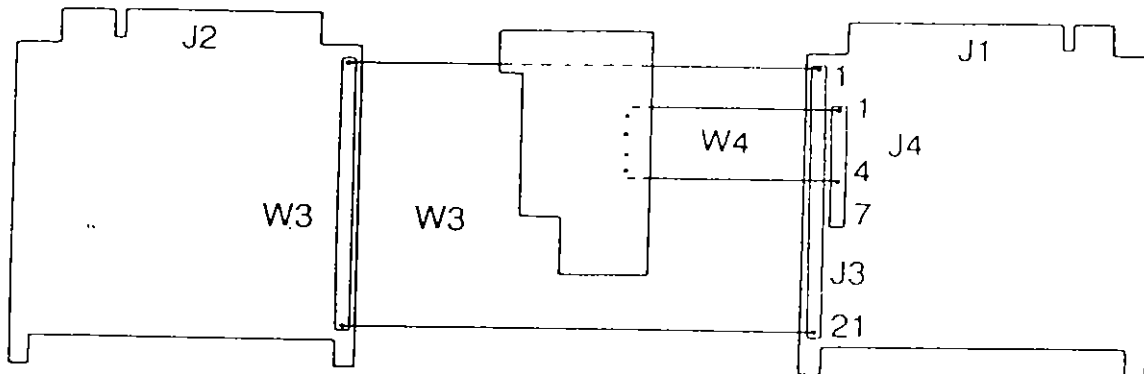


Figure 5-1 Board Interconnections

\*NOTE: There may be a socket for J3 position 22, but the flexible cable W3 must not be inserted into that socket.

5.1 MAIN BOARD CONNECTOR, P1  
(left to right looking at rear of case)

PIN CONNECTION	FUNCTION	NOTES
A	N/C	
B	N/C	
C	N/C	
D	N/C	
E	AC Power GND	
F	N/C	
H	Exc supply Return	Isolated Excitation Supply Isolated Excitation Supply (1 k source resistance)
J	Exc supply +	
K	+5 V	
L	Factory test	
M	DIGITAL GND	
N	DIGITAL GND	
P	N/C	
R	N/C	
S	$\overline{\text{RESET}}$	
T	DIGITAL GND	
U	N/C	
V	$\overline{\text{UP/DOWN}}$	

5.2  $\overline{\text{UP/DOWN}}$  SELECTION

The 6162A may be configured as an UP or a DOWN counter, capable of counting on rising or falling edges. Up or Down counting is achieved by a connection or logic level signal at the rear edge connector, P1 (see Figure 4-1).

The  $\overline{\text{Up/Down}}$  line, P1-pin V, is internally pulled up to +5 V through a 4.7k resistor. To configure the unit as a down counter, apply a low logic level or connect P1-pin V to digital ground (P1-pin T). The load is 4.7k to +5 V. To configure the unit as an up counter, apply a high logic level or leave P1-pin V open.

To prevent the 6162A's counter from making an incorrect jump when the voltage into the UP/DOWN input (P1-V) is changed use one of the following procedures:

1. Do not change this P1-V voltage while counting, OR
2. Use the following table as a guide to determine how long to wait after the input signal has made a counting edge transition before permitting the P1-V voltage to change. Refer to section 5.5 to determine if the rising or falling edge of the input signal is the counting edge. The times given in this table will be increased if the input signal magnitude is barely large enough to permit the 6162A to count it.

SIGNAL INPUT TERMINAL	SIGNAL CONDITIONER BOARD S3 JUMPER INSTALLED	TIME DELAY (milliseconds)
TB1-5	NONE	1
TB1-5	C	10
TB1-6	NONE	1
TB1-6	B	100

### 5.3 DECIMAL POINTS

Any one of five decimal points can be selected by installing a push-on jumper in the proper S1 position on the front display board. See Figure 5-2 for location.

Decimal Point Position	S1
X X X X X . X	A
X X X X . X X	B
X X X . X X X	C
X X . X X X X	D
X . X X X X X	E

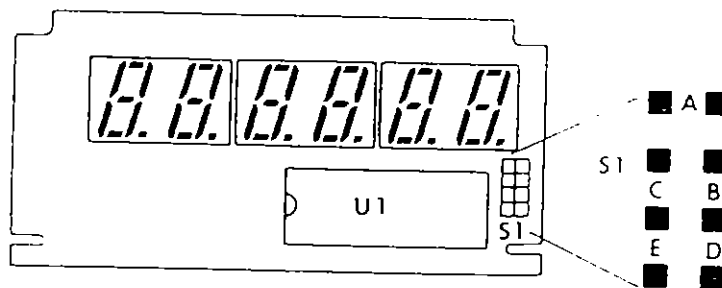


Figure 5-2 Display Board Jumper Locations

## 5.4 SIGNAL CONDITIONING

The 6162A contains a signal conditioning board with or without pre-divider. The conditioning circuitry is jumper-selectable to match the characteristics of the applied input signal. The three types of input signals accommodated are AC, DC pulse and Contact Closure.

The AC input is connected to TB1, terminal 5 and the DC input to TB1, terminal 6. Refer to Section 4.4 .

### IMPORTANT

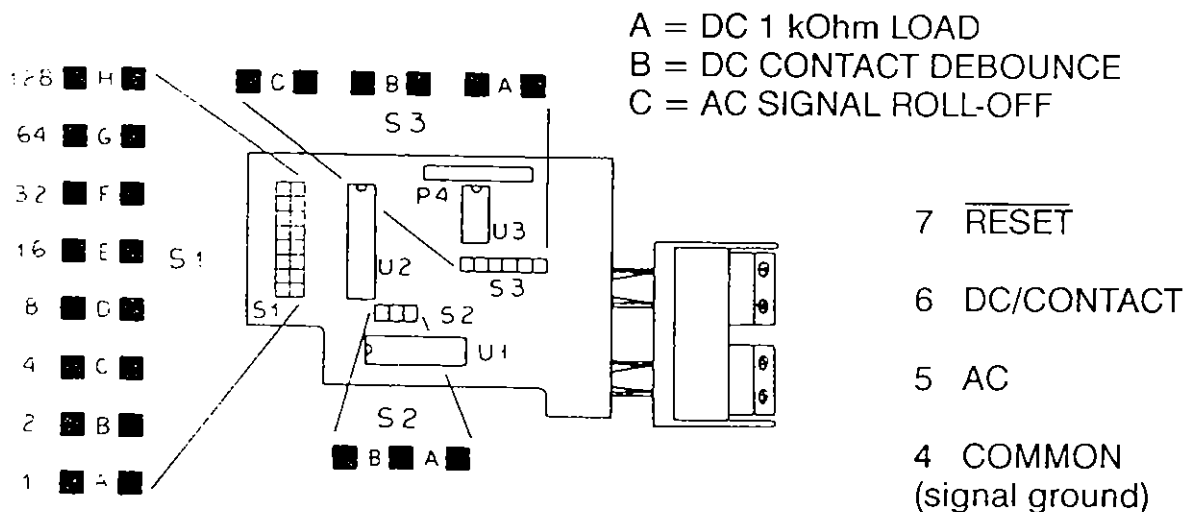
The unused input must be connected to Common(signal ground \*)  
(TB1, Terminal 4).

For each type of input signal, the addition of one or two jumpers on S3 can alter the signal conditioning characteristics. The effect of each and the location of S3 is described below.

Signal Conditioning	S3
**DC Contact 1 kOhm Load	A
DC Contact Debounce	B
AC Signal Roll-Off	C

\*NOTE Inside the 6162A signal ground is connected to digital ground. It is best, not to connect these two grounds together outside of the 6162A.

\*\*NOTE The maximum DC input voltage with jumper S3-A installed is +24 VDC. This 1 kOhm Load is usually used when the input TB1-6 is driven by an open-collector PNP transistor or a current source. It should not be used for a contact closure to ground input.



A = COUNT ON FALLING EDGE, WITHOUT PREDIVIDER  
B = COUNT ON RISING EDGE, WITHOUT PREDIVIDER

Figure 5-3 Signal Conditioner Jumper Locations

## 5.5 COUNTING EDGE

The 6162A may be configured to count on either the rising or the falling edge of the signal input. The edge is determined by the jumper position on the signal conditioning board pin group S2 (see Figure 5-3).

	Counting Edge	S2
Without Predivider	Falling Rising	A (factory-set) B
With Predivider	Falling Rising	B A

## 5.6 PREDIVIDER OPTION

If the instrument is fitted with the predivider option (PD), the input pulse stream may be divided by an integral number from 1 to 255 before being totalized. The division number is set by installing jumpers at S1 on the signal conditioner (see Figure 5-3 and Table 5-1). The S1 positions have binary-weighted values from 1 to 128 and the resulting divider value is the sum of the values selected.

For example, a predivision of 100 input pulses per count displayed requires jumpers at positions G, F and C ( $64 + 32 + 4$ ) of S1.

S1 Jumper Position	Binary Value
A	1
B	2
C	4
D	8
E	16
F	32
G	64
H	128

Table 5-1 Binary Values of Jumper Positions

For custom configuration, there are positions on the board for factory installed diodes to provide predivision binary-weighted values of 256, 512, 1024 and 2048. These diodes are shown within the inner dashed-line enclosure area shown in Figure 8-6. Capacitor C1 and the parts enclosed within the outer dashed-line are only installed when the predivider option (PD) is ordered. Solder switches A and B are also shown in that figure. For the standard totaliser, switch A is closed and B is open. When the predivider option (DP) is ordered these connections are reversed.

In calculating the total predivision, The binary-weighted values of the factory-installed diodes are treated just the same as the binary-weighted values of the diodes connected by the S1 jumpers. For example, a predivision of 1000 input pulses per count displayed requires factory-installed diodes with a value 512 and 256 plus jumpers at positions H, G, F, and D ( $512 + 256 + 64 + 32 + 8 = 1000$ ). There is no provision for the user to remove these factory-installed diodes; therefore, the user can only reconfigure the jumpers to increase the predivision set by the factory-installed diodes from 0 to 255 in steps of 1. For the above example, the factory-set predivision is 768 ( $256 + 512$ ); therefore, the user can change the total predivision from 768 to 1023 ( $768 + 255$ ) in steps of 1.

**IMPORTANT**

If the predivider option is present, a non-zero value of predivision **MUST** be used. If factory-installed predivision diodes are present, any configuration of S1 jumpers may be used. If these diodes are not present, at least one of these jumpers **MUST** be used. A predivision of 1 (jumper A only) would be acceptable.

## 5.7 DISPLAY AND OVERLOAD INDICATIONS

The 6-digit display uses leading zero blanking for the two most significant digits. If these two digits are zero while counting up and there is no overflow condition, they will be blank. This does not apply to counting down below zero (10's complement reading).

A round LED positioned to the left of the display lights to indicate an overflow condition on the next count after 999999 when counting up. It lights on the next count after BB0000 (B=blank) when counting down.

## 6.0 EXCITATION SUPPLY CONNECTIONS

The excitation supply is an isolated DC voltage available on the lower main board mating connector, P1.

Excitation Voltage	Connection
+ Output	P1-J
Output Return	P1-H

The output from this supply is galvanically isolated from the signal input to the counter. It may float up to 30 volts from signal common, but for most applications the excitation return (negative) terminal (P1-pin H) will be returned to the signal ground (TB1-terminal 4).

The output of the excitation supply is restricted to 20 mA at 12 volts by internal power dissipation, and restricted to 30 mA at 24 volts by regulation failure at low line. The regulator itself is protected by thermal shut-down if overloaded.

The output voltage is selected by a push-on jumper located at S3 on the main board (see Figure 6-1).

Nominal Excitation Voltage	S3	Max Current
24 VDC (18 V with C3 option)	No Jumper	30 mA (22 mA)
12 VDC	A	20 mA

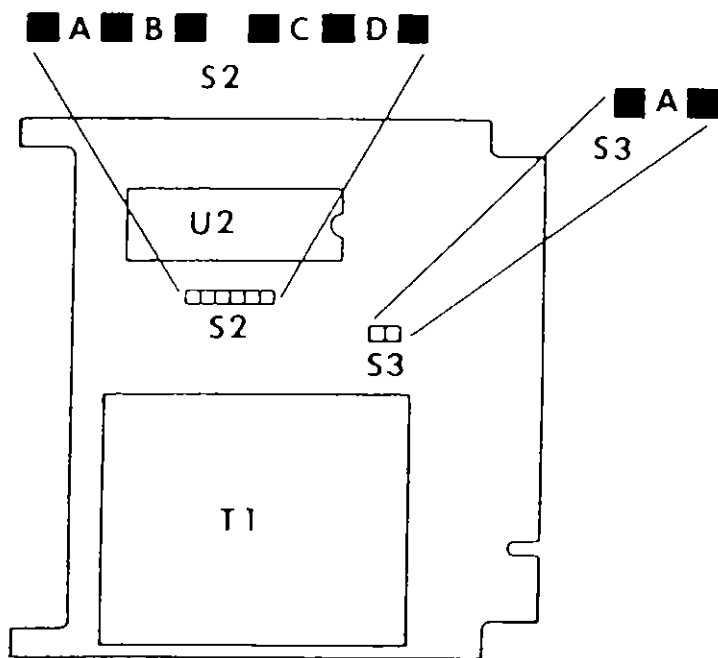


Figure 6-1 Main Board Jumper Locations

## 6.1 NAMUR TRANSDUCER CONNECTION

The excitation supply may be factory-configured for 8.5 volts output to satisfy NAMUR requirements by making the following changes on the main board.

1. Install a 3.92 kOhm\* resistor for R13.
2. Install jumper S3-A (see Figure 6-1).

Make connections as shown in Figure 6-2 below and install jumper S3-A on the signal conditioning board (see Figure 5-3).

\* 1/4 W commercial 1% metal film

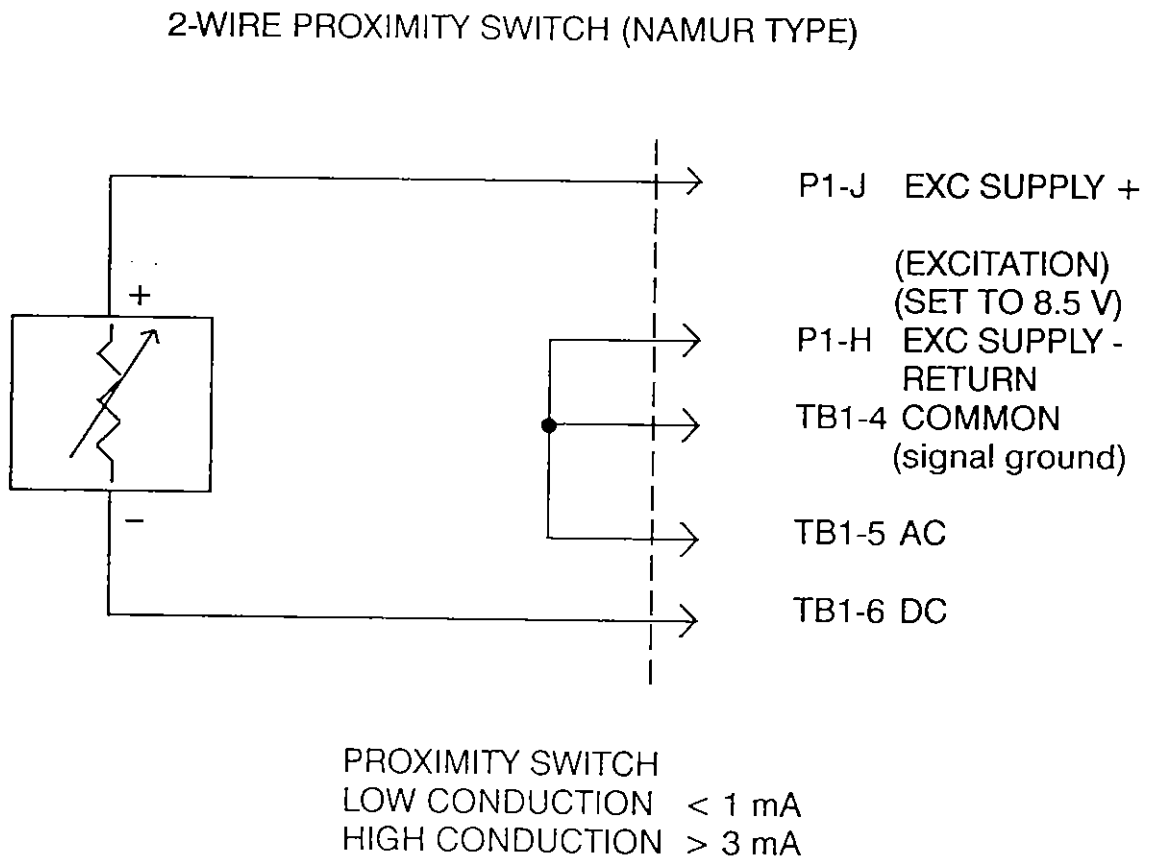


Figure 6-2 NAMUR Transducer Configuration

## 7.0 PARALLEL BCD OUTPUT OPTION (F6)

The F6 option provides six digits of buffered, non-isolated, gated and stored three-state BCD outputs, with  $\overline{\text{BCD HOLD}}$  and  $\overline{\text{DATA READY}}$  handshake signals. The latched and buffered three-state outputs are designed specifically for driving relatively low-impedance, high capacitance loads.

The low and high level drive capability plus the high impedance off state allow direct connection to bus-organized systems. In the addressed mode, the BCD outputs can be connected to the bus with a jumper-selected address from 0 to 15.

The positive-true BCD logic levels can drive  $\pm 6.0$  mA (15 LS-TTL units loads) each, and are TTL/CMOS (5 V) compatible with remote data processing devices such as digital setpoint controllers (Newport models 871, 872), printers (Newport 820A, 804), remote displays (Newport models 6152, 6153), programmable controllers and computers.

Because the BCD outputs are Newport bus compatible, a Model 320 Bus Controller and an 820A printer can be interfaced with up to fifteen three-state compatible instrument. The BCD output is not isolated from the signal input, it is critical that only one ground be introduced into the overall system. Therefore, the readout ground must be in common with the printer ground and in common with the sensor power supply ground (if the sensor requires a separate power supply). These are all tied together; and then they can be tied to earth ground at one point, thereby establishing earth ground as the ground reference for all the instruments in the system.

The BCD outputs are normally available in parallel, but when interfacing to programmable controllers, computers or other devices with limited input ports, the F6 may be reconfigured to multiplex three eight-bit bytes of information on an eight-bit bus using three strobe inputs.

The  $\overline{\text{BCD HOLD}}$  (handshake input) line, when brought low, initiates the sequence of capturing and storing the current count of the TOTALISER and multiplexing this value into the three-state output latches. If the BCD OPTION is already addressed with its jumper preset address when this sequence has been completed, the  $\overline{\text{DATA READY}}$  (handshake output) line will go low to signal this completion.

## 7.1 PARALLEL BCD OUTPUT SPECIFICATIONS

Accuracy: Same as basic instrument specifications

### Digital Inputs:

BCD HOLD plus the address  
and strobe lines B1, B2, B4, B8,  
LS STROBE, MID STROBE, and  
MS STROBE

Logical '0'	0 to 0.9 V
Logical '1'	+3.7 V to +5.25 V
Input Load	10 k pull-up resistor to + 5 V

### Digital Outputs:

#### BCD DATA

Logical '0'	0.33 V maximum at 6 mA
Logical '1'	3.8 V minimum at 6 mA (4.3 V minimum at 20 $\mu$ A)
Hi-Z state	$\pm 20$ $\mu$ A maximum at 0 V or + 4.5 V applied

#### DATA READY\*

Logical '0'	0.5 V maximum at 13 mA
Logical '1'	There is an 8.25 kOhm 1% pull-up resistor to +5 V

Access time with  
BCD HOLD/DATA READY  
handshake:

50 mS max from BCD HOLD high to low transition  
to valid data

Power (non-isolated): Supplied by host meter

Environmental: Same as basic meter

\*NOTE: This output circuit with the 8.25 kOhm pull-up resistor will permit up to 15 of these BCD OUTPUT option unit to be connected in parallel and still drive 10 LS-TTL unit loads or CMOS loads with  $\pm 10$   $\mu$ A total load current within approx. 12 microseconds. It can also drive CMOS loads with  $\pm 60$   $\mu$ A total load current more slowly. Due to the limited pull-up current available (through the 8.25 kOhm resistor), this DATA READY output circuit can not drive a load which consists of a mixture of both TTL and CMOS inputs.

## 7.2 BCD OUTPUT CONNECTIONS

Parallel BCD output interface connections are made through a 25/50 pin double row connector, P2, on the rear of the board (see Figure 4-1). This connector is available with solder-eyelet connections (part number D50S) or mass-termination connections (part number D50M).

P2 CONNECTOR (Left to right, viewing the rear of the case)				
LOWER ROW			UPPER ROW	
	N/C	L1	U1	N/C
	N/C	L2	U2	N/C
	N/C	L3	U3	N/C
	N/C	L4	U4	N/C
	BCD 400 k	L5	U5	BCD 800 k
	BCD 100 k	L6	U6	BCD 200 k
	Ground	L7	U7	N/C
	BCD 40 k	L8	U8	BCD 80 k
	BCD 10 k	L9	U9	BCD 20 k
	BCD 4 k	L10	U10	BCD 8 k
	BCD 1 k	L11	U11	BCD 2 k
	N/C	L12	U12	N/C
	BCD 400	L13	U13	BCD 800
	BCD 100	L14	U14	BCD 200
	BCD 40	L15	U15	BCD 80
	BCD 10	L16	U16	BCD 20
	BCD 4	L17	U17	BCD 8
	BCD 1	L18	U18	BCD 2
	Ground	L19	U19	N/C
	<u>DATA READY</u>	L20	U20	<u>FACTORY TEST</u>
	* Spare	L21	U21	<u>BCD HOLD</u>
	N/C	L22	U22	N/C
	<u>(MS STROBE)</u> (Addr B4) B4	L23	U23	B8 (Addr B8)
	<u>(LS STROBE)</u> (Addr B1) B1	L24	U24	B2 (Addr B2) <u>(MID STROBE)</u>
	N/C	L25	U25	N/C

\* In a non-Newport bus-compatible system, L21 may be used for a 5 V output at 5 mA maximum. To configure the unit for 5 V output on this pin, close solder switch A located on the component side of the F6 board near pin U25.

### 7.3 BCD CONFIGURATION SELECTION

The F6 may be configured for all 24 outputs available in parallel (24-bit parallel mode) or 8 outputs active at a time, under control of three strobe lines (8-bit parallel mode). Refer to Section 7.3.1 and 7.3.2 for the 24-bit parallel mode; refer to Section 7.3.1 and 7.3.2 for the strobed 8-bit parallel mode. The different configurations are made with push-on jumpers. For jumpers A through H, one of the jumper combinations shown in table 7-1 must always be used regardless of the mode of operation. For the 24-bit parallel mode, use only jumpers I, J, and M plus one set of jumpers shown in table 7-1. For the 8-bit parallel mode, use jumpers A, B, E, F, K, L, and N only. Figure 7-1 illustrates jumper locations.

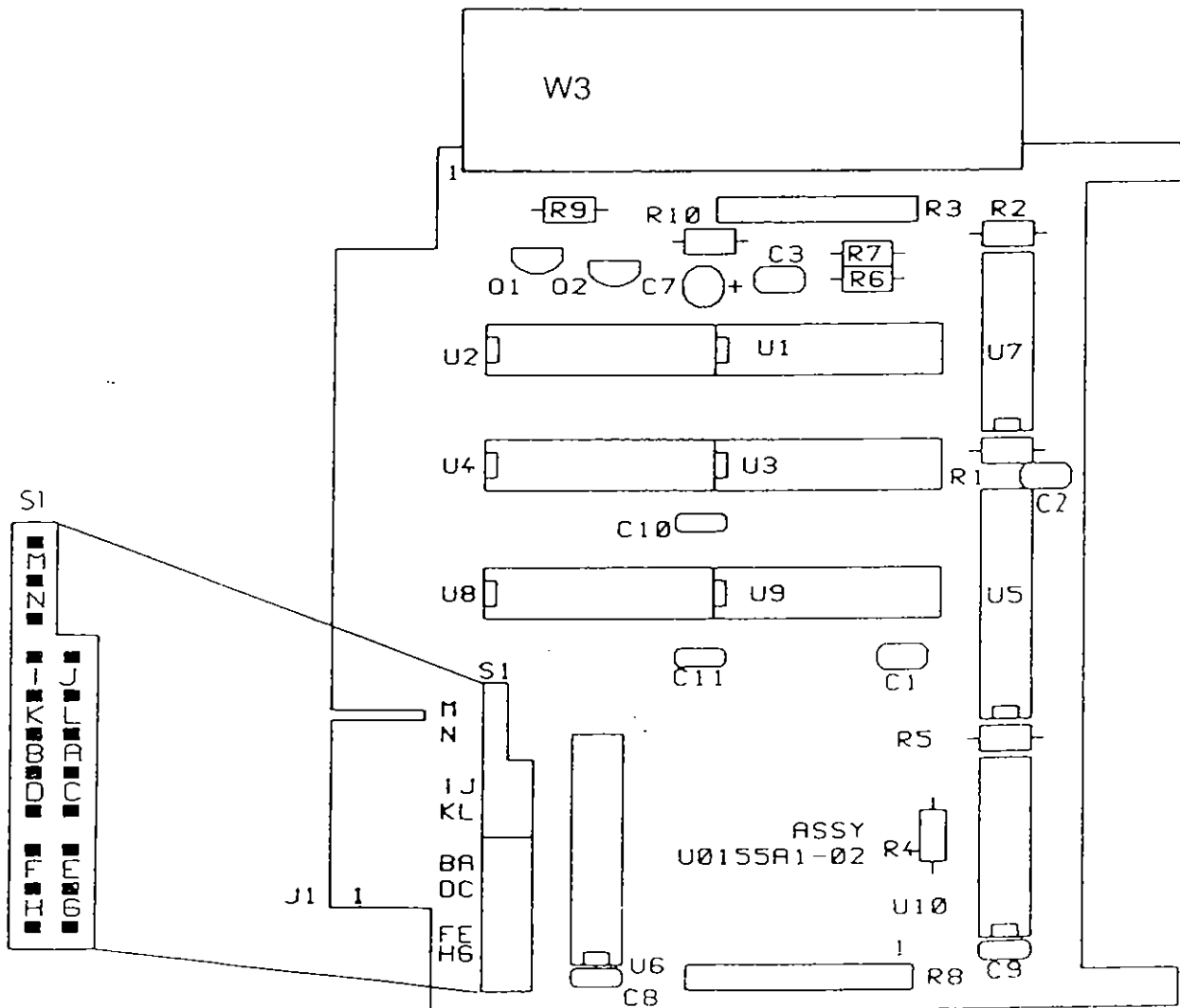


Figure 7-1 F6 Jumper Locations

### 7.3.1 24-Bit Parallel Mode

In this mode, all 24 BCD outputs are available simultaneously. These are three-state outputs that may be controlled in one of the following ways:

1. Put into a high-impedance state until enabled by the address lines. This is useful for connecting the BCD outputs to a bus with other BCD outputs.
2. Active continuously for point-to-point connection.

Either way, the 24-Bit Parallel mode is configured by installing jumpers S1 jumpers I, J, and M on the F6 board (refer to figure 7-1).

Next, the 4-bit binary address of the board must be jumpered according to Table 7-1. When the selected address is matched by the data on the four address lines B8, B4, B2 and B1, the 24 parallel BCD outputs are made active (in their low impedance state). When the selected address and the address data do not match, the 24 BCD outputs are in their high-impedance state.

BINARY ADDRESS B8 B4 B2 B1	DECIMAL EQUIVALENT		JUMPER POSITIONS (Figure 7-1)
	POS TRUE	NEG TRUE	
0 0 0 0	0	15	C, D, G, H
0 0 0 1	1	14	C, D, F, G
0 0 1 0	2	13	A, D, G, H
0 0 1 1	3	12	A, D, F, G
0 1 0 0	4	11	B, C, G, H
0 1 0 1	5	10	B, C, F, G
0 1 1 0	6	9	A, B, G, H
0 1 1 1	7	8	A, B, F, G
1 0 0 0	8	7	C, D, E, H
1 0 0 1	9	6	C, D, E, F
1 0 1 0	10	5	A, D, E, H
1 0 1 1	11	4	A, D, E, F
1 1 0 0	12	3	B, C, E, H
1 1 0 1	13	2	B, C, E, F
1 1 1 0	14	1	A, B, E, H
1 1 1 1	15	0	A, B, E, F

Table 4-1 BCD Address Configuration

If the 24 parallel BCD outputs are to be continuously active and not bussed together with other BCD data, but connected point-to-point only, then install a jumper for positive true address of 15 (jumpers A, B, E, F). The four address lines (B8, B4, B2, B1) should be left open so the internal pull-up resistors provide logic 1's on the open inputs.

If the 24 parallel BCD outputs are to be bussed with other BCD outputs, they must be in the high-impedance output state until the card is addressed. Assign the desired address to this F6 option board and add the corresponding jumpers shown in Table 7-1. The address lines B8, B4, B2, B1 can now be used to address the BCD output board when the outputs are to become active. If the bus-organized system uses only a few address values, all four of the address lines might not be required. An open address line is left in the 1 state due to an internal pull-up resistor.

NOTE: Care must be taken to ensure that this parallel BCD output option is not put in its active (low impedance) state, by applying its preset address, while any other BCD output on the same bus is also active. Otherwise, its output stages could be damaged.

### 7.3.2 24-Bit Parallel Mode Handshaking

Following is the external system operation of the high output impedance to the BCD bus until addressed mode:

1. Bring the BCD HOLD input line low.
2. Wait 50 milliseconds (minimum).
3. Address the BCD OPTION with its jumper preset address.
4. Wait 4.0  $\mu$ seconds (minimum) (see NOTE in section 7.3.4).
5. Read the data on the BCD bus which is the representation of the TOTALISER count present within 15  $\mu$ seconds after the time BCD HOLD was brought low in step one above.
6. Change the address.
7. Bring the BCD HOLD input line high. This step is necessary so that in the future this line can be brought low again to capture the latest value of the TOTALISER count.

Alternative external system operation:

1. Bring the BCD HOLD input line low and address the BCD OPTION with its jumper preset address.
2. Wait until the DATA READY output line goes low (within 50 milliseconds).
3. Wait 4.0  $\mu$ seconds (minimum) (see NOTE in section 7.3.4).
4. Read the data on the BCD bus.
5. Bring the BCD HOLD input line high and change the address.

Following is the external system operation of the low output impedance to the BCD bus continuously active mode:

1. Bring the  $\overline{\text{BCD HOLD}}$  input line low.
2. Wait until the  $\overline{\text{DATA READY}}$  output line goes low (within 50 milliseconds).
3. Wait 4.0  $\mu\text{seconds}$  (see NOTE in section 7.3.4).
4. Read the data on the BCD bus.
5. Bring the  $\overline{\text{BCD HOLD}}$  input line high. (The BCD OPTION is now putting data on the BCD bus which is sometimes erroneous, and the external system must ignore this data).

### 7.3.3 8-Bit Parallel Mode

In this mode, the least significant digits BCD outputs are made active with  $\overline{\text{LS STROBE}}$  line B1 (P2-L24), the next two most significant digits BCD outputs with  $\overline{\text{MID STROBE}}$  line B2 (P2-U24), and the two most significant digits BCD outputs with  $\overline{\text{MS STROBE}}$  line B4 (P2-L23). The strobe polarity is:

Low level (0) strobe = 8 BCD outputs active (low impedance)  
High level (1) strobe = 8 BCD outputs high-impedance.

The 8-Bit Parallel mode is configured by installing jumpers A, B, E, F, K, L, and N on the BCD option board. Remove all jumpers from the S1 pin group. The B8 address line (P2-U23) must be kept open or at high logic level.

In this mode, the BCD output board cannot be addressed as it can in the 24-Bit Parallel mode, so Table 7-1 does not apply.

The purpose of the 8-Bit Parallel mode is for point-to-point connection to instruments such as process-controllers that accept BCD data 8 bits at a time under control of three strobe lines. The two least significant, next two most significant, and most two significant digits BCD outputs are connected in parallel and each set is made active alternately with the strobe lines while the data is read synchronously. This reduces the number of BCD output data lines from 24 to 8 that must be cabled.

P2 TERMINALS TO BE CONNECTED TOGETHER FOR THE 8-BIT PARALLEL MODE							
STROBES	MS (P2-L23) : MID (P2-U24) : LS (P2-L24)						RELATIVE
DIGITS	D6	D5	D4	D3	D2	D1	WEIGHTS
P2-	U5-----		U10-----		U15		8
P2-	L5-----		L10-----		L15		4
P2-	U6-----		U11-----		U16		2
P2-	L6-----		L11-----		L16		1
P2-	U8-----		U13-----		U17		8
P2-	L8-----		L13-----		L17		4
P2-	U9-----		U14-----		U18		2
P2-	L9-----		L14-----		L18		1

NOTE: Care must be taken to ensure that only one of the three strobe lines B1, B2, and B4 is low at one time and that none may go low until the other two have been high for at least 200 nanoseconds (0.20  $\mu$ seconds). This is necessary to prevent damage to the output stages caused by simultaneously activating two of them connected to each other (i.e. connected in parallel).

### 7.3.4 8-Bit Parallel Mode Handshaking

Following is the external system operation of the 8-bit parallel mode handshaking:

1. Bring the  $\overline{\text{BCD HOLD}}$  input line low. (All strobe lines should be high initially).
2. Wait 50 milliseconds (minimum).
3. Bring one of the strobe lines low (e.g.  $\overline{\text{LS STROBE}}$  (=B1=P2-pin L24)). The order in which the strobe lines are brought low is determined by the user.
4. Wait 4.0  $\mu\text{seconds}$  (minimum) (see NOTE below).
5. Read the data on the BCD bus. The particular strobe line which is low at the time determines which digits this data represents.
6. Bring this first strobe line high.
7. Wait 0.2  $\mu\text{seconds}$  (minimum).
8. Repeat steps 3-7 for the next strobe line.
9. Repeat steps 3-6 for the last strobe line.
10. Bring the  $\overline{\text{BCD HOLD}}$  input line high.

Alternative external system operation:

1. Bring the  $\overline{\text{BCD HOLD}}$  input line low. (All strobe lines should be high initially).
2. Wait until the  $\overline{\text{DATA READY}}$  output line goes low (within 50 milliseconds).
3. Bring one of the strobe lines low (e.g.  $\overline{\text{LS STROBE}}$  (=B1=P2-pin L24)). The order in which the strobe lines are brought low is determined by the user.
4. Wait 4.0  $\mu\text{seconds}$  (minimum) (see NOTE below).
5. Read the data on the BCD bus. The particular strobe line which is low at the time determines which digits this data represents.
6. Bring this first strobe line high.
7. Wait 0.2  $\mu\text{seconds}$  (minimum).
8. Repeat steps 3-7 for the next strobe line.
9. Repeat steps 3-6 for the last strobe line.
10. Bring the  $\overline{\text{BCD HOLD}}$  input line high.

**NOTE:** This 4.0  $\mu\text{second}$  of required "wait" time is based upon a maximum bus capacitance of 1500 pF to ground and a total of 750 pF to the other bus conductors and is measured from the time that address lines reach the logic levels specified in section 7-1. For a capacitance of 150 pF to ground and a total of 75 pF to other conductors, it would be 6.0  $\mu\text{seconds}$ . The 10 k pull-up resistors to +5 V will usually permit LS-TTL circuits to drive these address or strobe lines, provided they are not also driving any TTL or LS-TTL inputs; however, there will be an added time delay to pull the high logic levels of these circuits to the +3.7 V specified in section 7-1. If the address line capacitance to ground were 1500 pF and the total capacitance to other conductors were 750 pF, this added time could be approximately 100  $\mu\text{seconds}$ .

## 7.4 BCD HOLD AND DATA HOLD

The BCD HOLD (handshake input) line, when brought low, initiates the sequence of capturing and storing the current count of the TOTALISER and multiplexing this value into the three-state output latches. If the BCD OPTION is already addressed with its jumper preset address when this sequence has been completed, the DATA READY (handshake output) line will go low to signal this completion.

## 7.5 HANDSHAKING DETAILS

There are two individual lines, BCD HOLD input and DATA READY output, and two groups of lines, address lines (B1, B2, B4, and B8) and strobe lines (LS STROBE, MID STROBE, and MS STROBE) involved in handshaking. The address and strobe lines share terminals on connector P2.

When the parallel BCD output option is configured for the 24-bit parallel mode the following handshaking sequence occurs.

1. The BCD HOLD input line is brought low.
2. Within a maximum of 15.0  $\mu$ seconds, the current count in the TOTALISER will be captured and saved.
3. Within a maximum of 50 milliseconds (22 milliseconds typical), the BCD data corresponding to that count will have been multiplexed and stored in the output latches. The actual time of completion of this multiplexing and storing is signaled by the DATA READY output line going low if the BCD OPTION is addressed with its jumper preset address.
4. From this time until the BCD HOLD input line is opened or brought to a high logic level, the data in the output latches is valid and unchanging. If the BCD OPTION is already addressed with its preset address, this output latch valid data is also available on the BCD bus and the DATA READY output line will be low. If the BCD OPTION has not been addressed, the output of these latches will be in their high impedance state and the DATA READY output line will be high. If it was not addressed and then becomes addressed, this valid BCD data will be put on the BCD bus within 4.0  $\mu$ seconds (see NOTE in section 7.3.4) and the DATA READY output line will go low within 5  $\mu$ seconds.
5. When the BCD HOLD input line goes high, the system will return to its standby mode. The DATA READY output will be high and the BCD OPTION will be continuously putting TOTALISER count data into the output latches. However since the input counts to the TOTALISER can occur anywhere within the internal multiplexer cycle, this data will not be a reliable indication of the current TOTALISER count. (This error increases with count frequency.) This latch data will be output to the BCD bus if and only if the BCD OPTION is addressed with its preset address.

When the parallel BCD output option is configured for the 8-bit parallel mode, the handshaking sequence is similar to the 24-bit mode with the following exceptions:

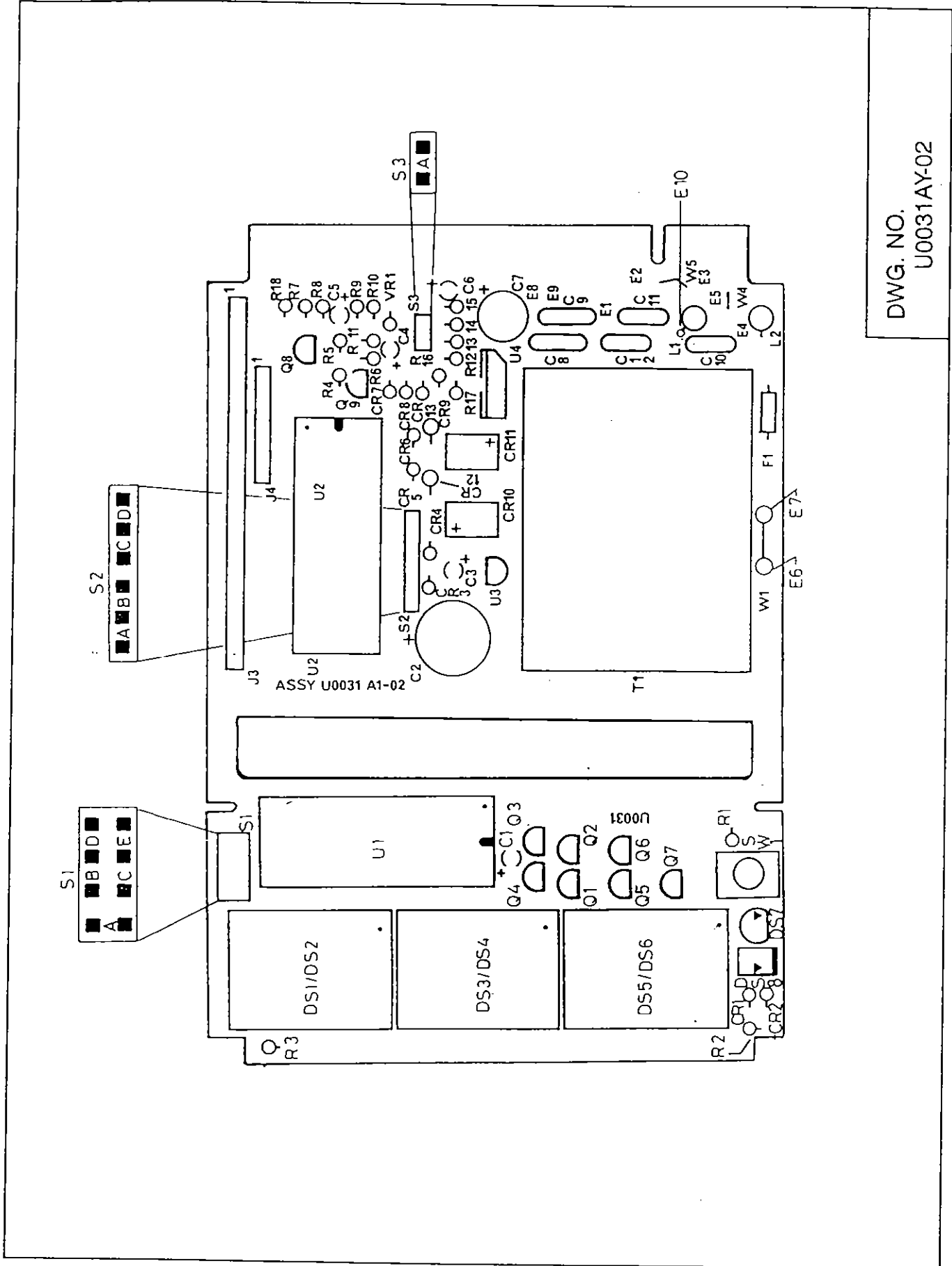
1. In the 24-bit mode, the three-state output latches for all six digits were controlled by the total address applied to the BCD OPTION. Thus if the logic levels of all the address lines matched those preset by S1 jumpers A-H, the outputs of all latches were in their active (low impedance) state; and the data in these latches was put on the BCD bus. If the applied Address did not match the jumper preset address, all of those latches output states were high impedance and the BCD bus was left floating. No other logic was involved.

In the 8-bit mode these six latches are divided into three groups of two latches each. The output state of each group of two latches is controlled by a single strobe line--one of the address lines. Thus if the  $\overline{\text{LS STROBE}}$  line (B1) is low the outputs of the latches for the two least significant digits (D1 and D2) are in their active (low impedance) state. Otherwise, they are in their high impedance state. *Note, that since the outputs of these three groups are all externally wired to the same eight wires, to avoid damage to the BCD OPTION it is necessary to have only one of these strobe lines low at any one time and none may go low until both of the other two have been at a high logic level for at least 200 nanosecond (0.20  $\mu$ seconds). There is no logic within the BCD OPTION to assure this safe condition; therefore, it is up to the user to observe this caution.*

2. In the 24-bit mode, the  $\overline{\text{DATA READY}}$  output line was low if and only if:
  - a. The  $\overline{\text{BCD HOLD}}$  input line was low and had been low long enough (50 milliseconds max) for the TOTALISER count to have been captured, stored and multiplexed into all the output latches AND
  - b. The address applied to the BCD OPTION matched the jumper preset address.

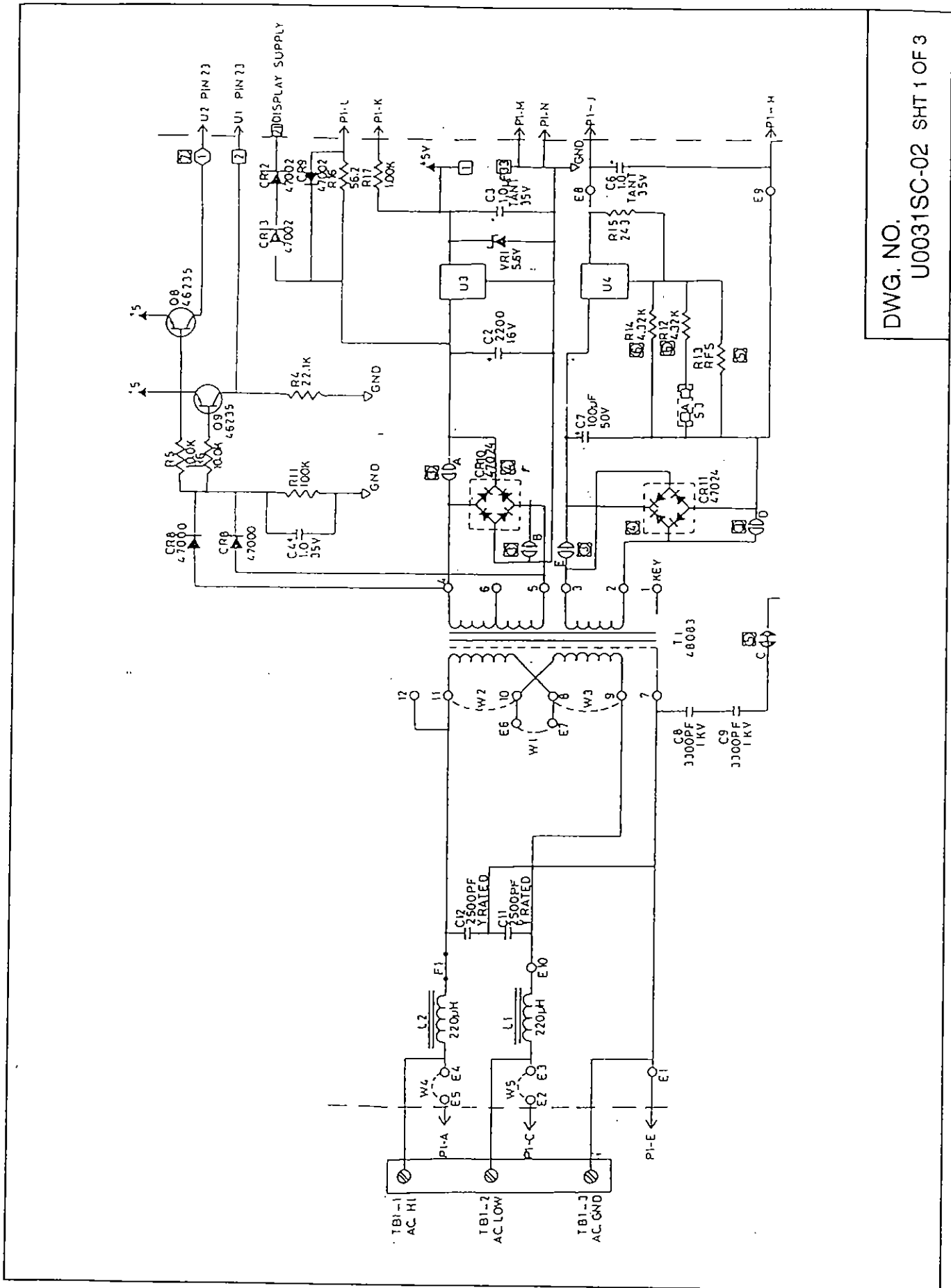
In the 8-bit mode, these conditions for which the  $\overline{\text{DATA READY}}$  output line would be low are identical; but the consequences are somewhat different. Since three different applied addresses are required to output all of the BCD data on the BCD bus, the  $\overline{\text{DATA READY}}$  output line cannot be low for all three. However, its timing information may still be used. In both the 24- and 8-bit modes, the timing information yielded by the  $\overline{\text{DATA READY}}$  output line going low can be used by external systems which do not have the capability to time the 50 milliseconds after the  $\overline{\text{BCD HOLD}}$  input line is brought low until valid BCD data may be read.

In the 8-bit mode, only S1 jumpers A, B, E, F, K, L, and N should be used. Also P2-pin U23 (address line B8) should be left unconnected. In this configuration, when all of the strobe lines are high (BCD bus floating), the applied address will match the preset address and the  $\overline{\text{DATA READY}}$  output line will go low when valid unchanging data is stored in the output latches. Thus, this going low of the  $\overline{\text{DATA READY}}$  output line can be used in step 2 of the alternative operation shown in section 7.3.4.



DWG. NO.  
U0031AY-02

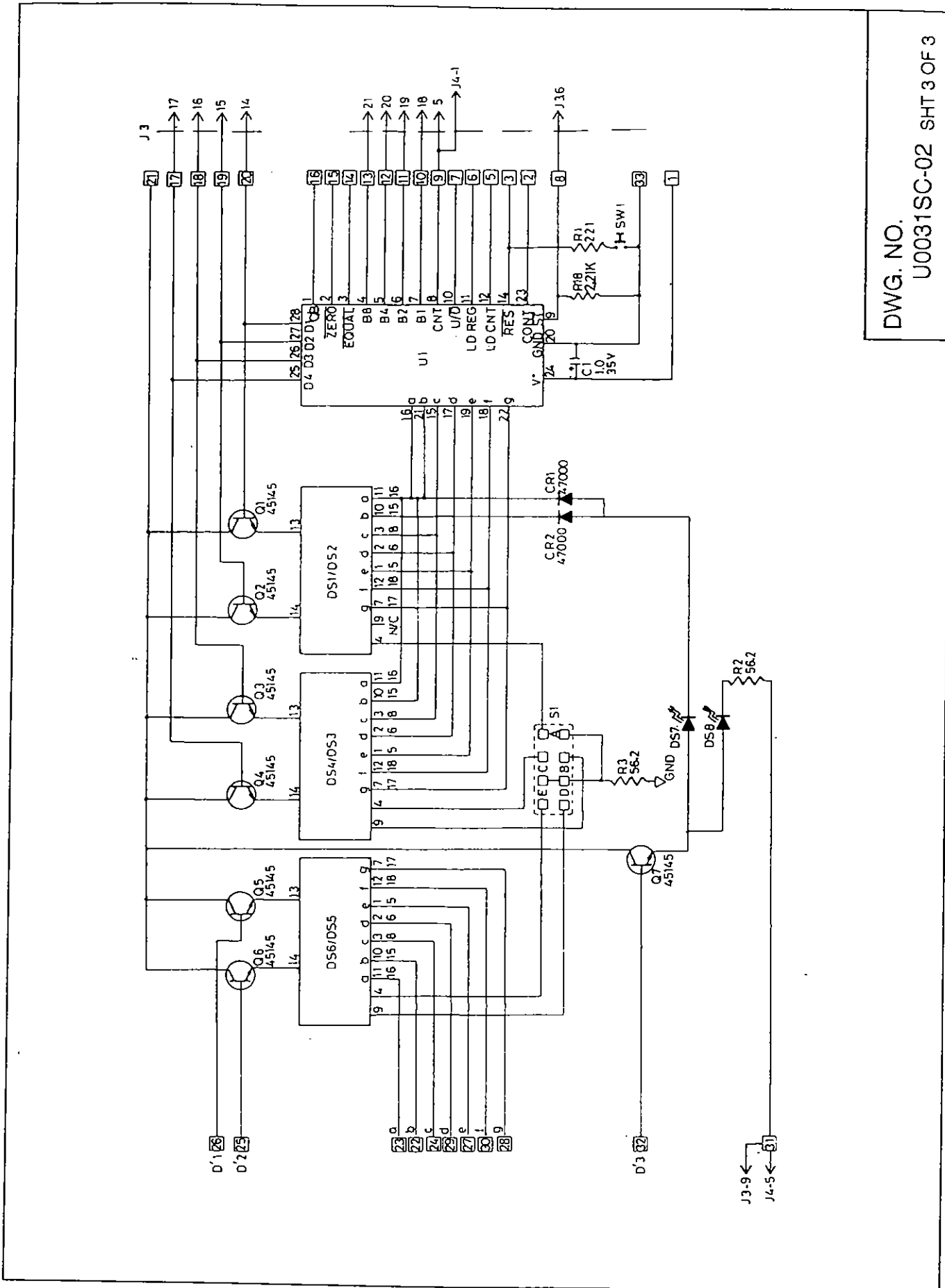
Figure 8-1 6162A Main Assembly Diagram



DWG. NO.  
U0031SC-02 SHT 1 OF 3

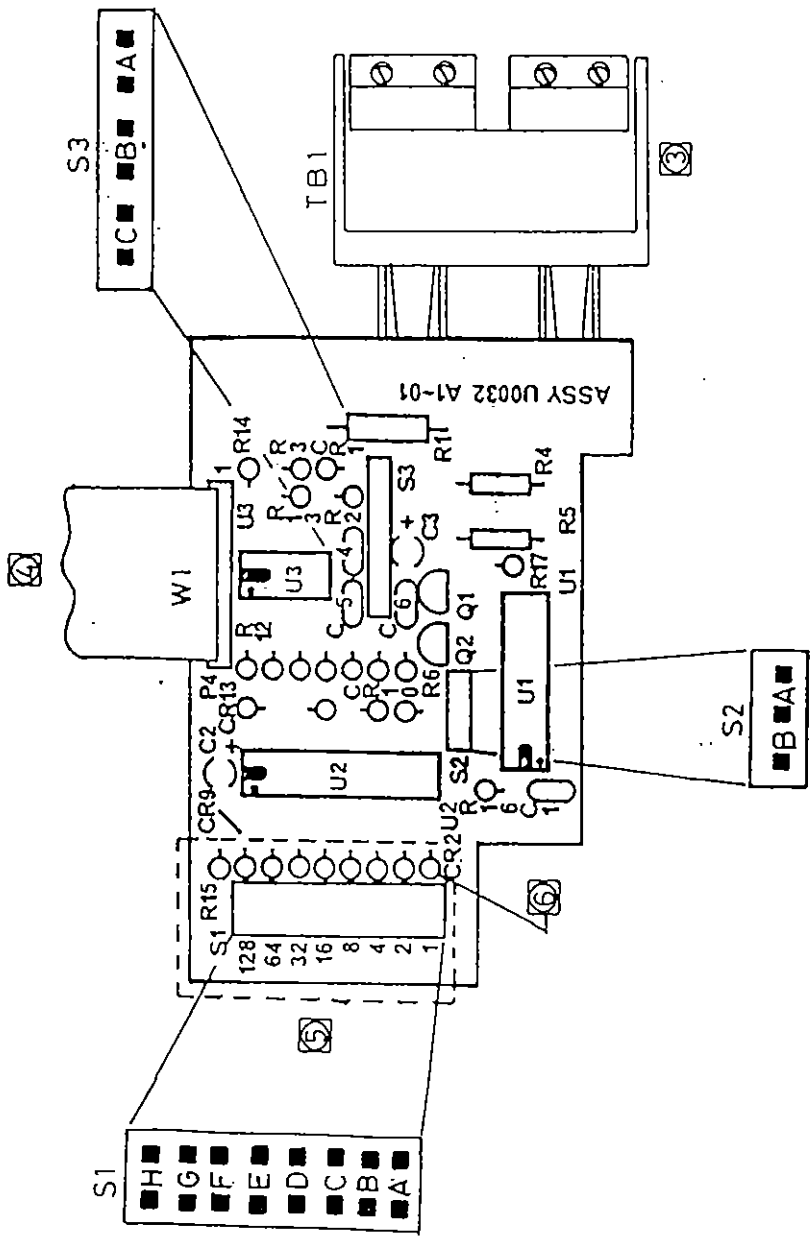
Figure 8-2 6162A Schematic Diagram (1 of 3)





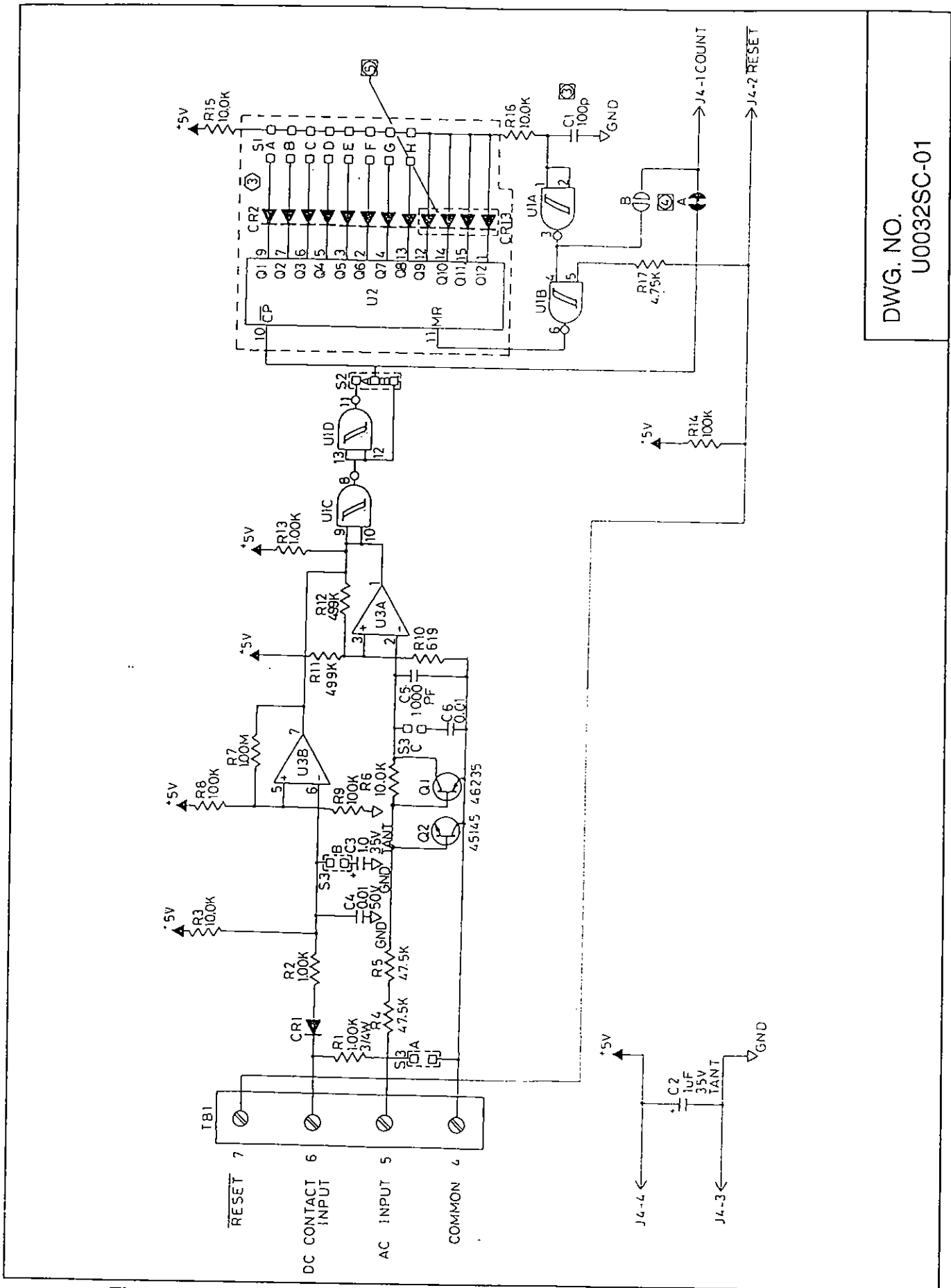
DWG. NO. U0031SC-02 SHT 3 OF 3

Figure 8-4 6162A Schematic Diagram (3 of 3)



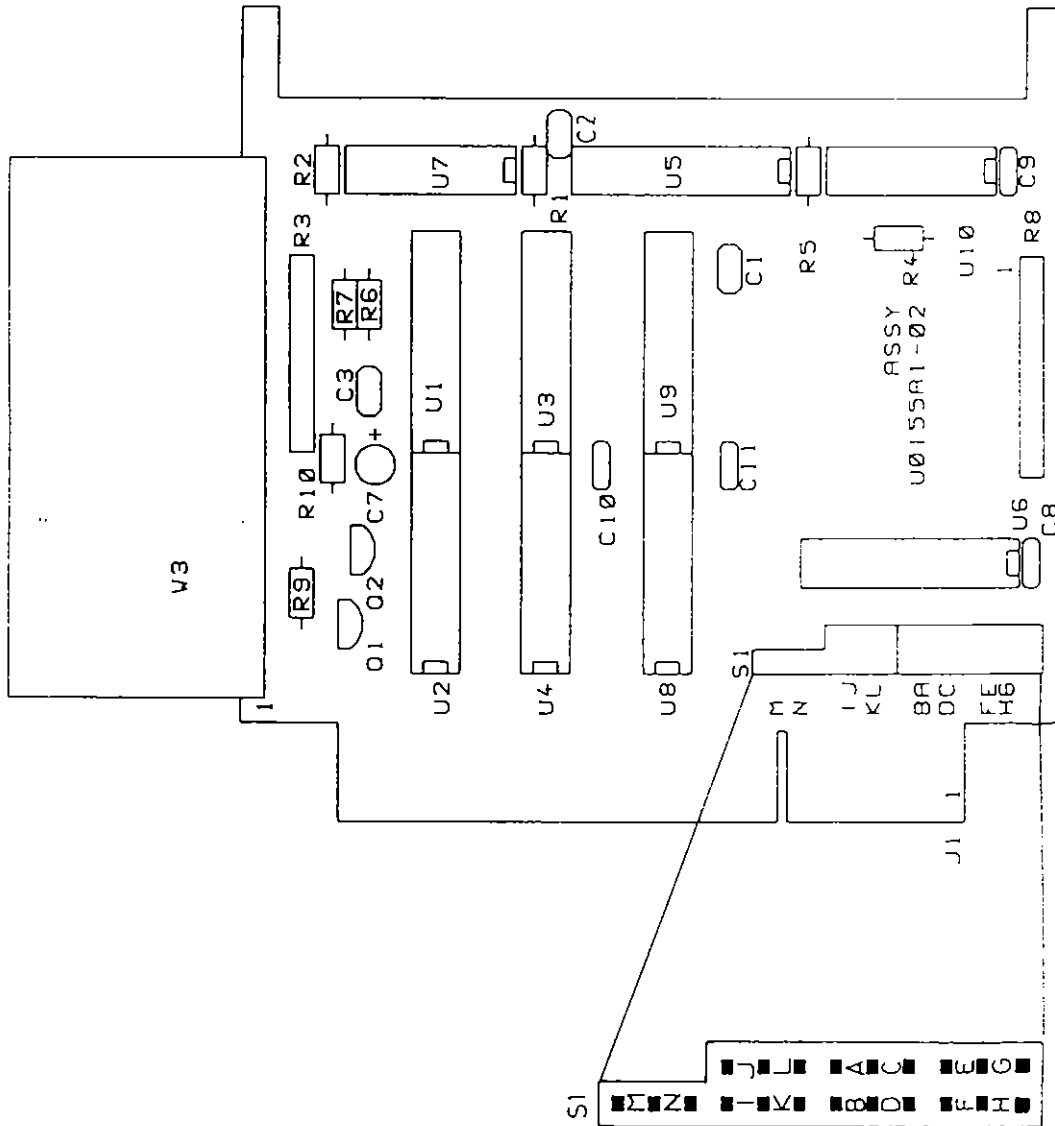
DWG. NO.  
U0032AY-01

Figure 8-5 Signal Conditioner Assembly Diagram (with PD Option)



DWG. NO.  
U0032SC-01

Figure 8-6 Signal Conditioner Schematic Diagram (with PD Option)



DWG. NO.  
U0155AY-02

Figure 8-7 Parallel BCD Assembly Diagram

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